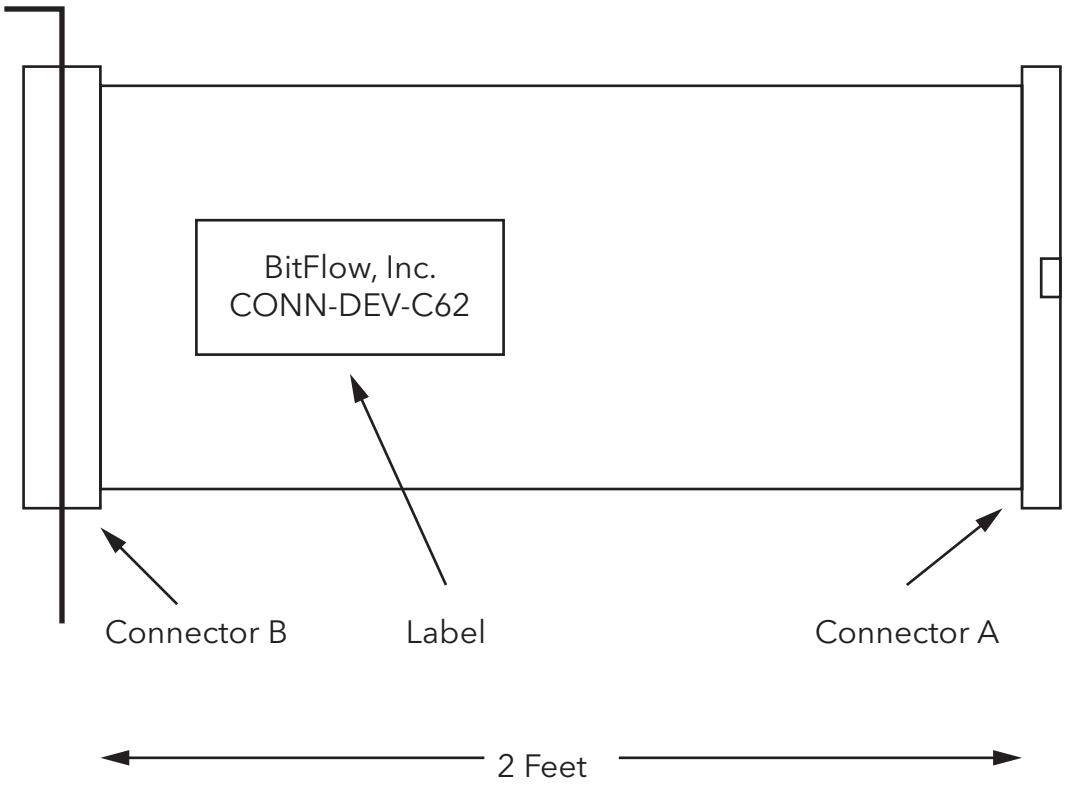
BitFlow Cable - CONN-DEV-C62
Revision 1.1

Purpose

This cable brings all of the I/O connections from the internal mass-terminated connector to a D-sub connector in a PC slot. This cable works with most modern frame grabbers, including but not limited to the Neon-CLQ, Karbon-CL, Karbon-CXP, Cyton-CXP and Axion-CL.

Note: This cable replaces the CONN-KBN-IO.

Diagram



Construction

Connector A is a 60 pin mass termination connector with a single center key. The cable at connector A is on the same side like the polarizing key. There is no strain relief on A.

Connector B is a female three row, 62-pin D-sub. It is mounted to the bracket with hex screws. Suggested part for connector B is AMP 748568-1.

The PC bracket is GOMPF 9047-0044. On connector B put a sticker with the marking:

BitFlow, Inc.
CONN-DEV-C62

Wiring between connectors A and B is one-to-one: pin 1 of A connects to pin 1 of B, etc.

At Connector B, the flat cable must be split and wired to individual pins.

Pinout

See following pages.

Connector B	NEO-PCE-CLQ	KBN-PCE-CL2-D	KBN-PCE-CL2-F	KBN-PCE-CL4-D	KBN-PCE-CL4-F	KBN-PCE-CXP4	CTN-PC2-CXP2/4 AXN-PC2-1xE/2xE
1	VFG0_TRIGGER+	VFG0_TRIGGER+	VFG0_TRIGGER+	VFG0_TRIGGER+	VFG0_TRIGGER+	VFG0_TRIGGER+	VFG0_TRIGGER+
2	VFG0_TRIGGER-	VFG0_TRIGGER-	VFG0_TRIGGER-	VFG0_TRIGGER-	VFG0_TRIGGER-	VFG0_TRIGGER-	VFG0_TRIGGER-
3	VFG0_TRIGGER_TTL	VFG0_TRIGGER_TTL	VFG0_TRIGGER_TTL	VFG0_TRIGGER_TTL	VFG0_TRIGGER_TTL	VFG0_ENCODERA+	VFG0_ENCODERA+
4	VFG0_ENCODERA_TTL	VFG0_TRIGGER_OPTO_K	VFG0_TRIGGER_OPTO_K	VFG0_TRIGGER_OPTO_K	VFG0_TRIGGER_OPTO_K	VFG0_ENCODERA-	VFG0_ENCODERA-
5	VFG0_GPOUT0_TTL	VFG0_TRIGGER_OPTO_A	VFG0_TRIGGER_OPTO_A	VFG0_TRIGGER_OPTO_A	VFG0_TRIGGER_OPTO_A	VFG0_ENCODERB+	VFG0_ENCODERB+
6	VFG0_GPOUT1_TTL	GND	GND	GND	GND	VFG0_ENCODERB-	VFG0_ENCODERB-
7	VFG1_TRIGGER+	VFG0_ENCODER+	VFG0_ENCODER+	VFG0_ENCODER+	VFG0_ENCODER+	VFG1_TRIGGER+	VFG1_TRIGGER+
8	VFG1_TRIGGER-	VFG0_ENCODER-	VFG0_ENCODER-	VFG0_ENCODER-	VFG0_ENCODER-	VFG1_TRIGGER-	VFG1_TRIGGER-
9	VFG1_TRIGGER_TTL	VFG0_ENCODER_TTL	VFG0_ENCODER_TTL	VFG0_ENCODER_TTL	VFG0_ENCODER_TTL	VFG1_ENCODERA+	VFG1_ENCODERA+
10	VFG1_ENCODERA_TTL	VFG0_ENCODER_OPTO_K	VFG0_ENCODER_OPTO_K	VFG0_ENCODER_OPTO_K	VFG0_ENCODER_OPTO_K	VFG1_ENCODERA-	VFG1_ENCODERA-
11	VFG1_GPOUT0_TTL	VFG0_ENCODER_OPTO_A	VFG0_ENCODER_OPTO_A	VFG0_ENCODER_OPTO_A	VFG0_ENCODER_OPTO_A	VFG1_ENCODERB+	VFG1_ENCODERB+
12	VFG1_GPOUT1_TTL	GND	GND	GND	GND	VFG1_ENCODERB-	VFG1_ENCODERB-
13	VFG2_TRIGGER+	VFG0_GPIN0_TTL	VFG0_GPIN0_TTL	VFG0_GPIN0_TTL	VFG0_GPIN0_TTL	VFG2_TRIGGER+	VFG2_TRIGGER+
14	VFG2_TRIGGER-	VFG0_GPIN1_TTL	VFG0_GPIN1_TTL	VFG0_GPIN1_TTL	VFG0_GPIN1_TTL	VFG2_TRIGGER-	VFG2_TRIGGER-
15	VFG2_TRIGGER_TTL	VFG0_GPIN2+	VFG0_GPIN2+	VFG0_GPIN2+	VFG0_GPIN2+	VFG2_ENCODERA+	VFG2_ENCODERA+
16	VFG2_ENCODERA_TTL	VFG0_GPIN2-	VFG0_GPIN2-	VFG0_GPIN2-	VFG0_GPIN2-	VFG2_ENCODERA-	VFG2_ENCODERA-
17	VFG2_GPOUT0_TTL	VFG0_GPIN3+	VFG0_GPIN3+	VFG0_GPIN3+	VFG0_GPIN3+	VFG2_ENCODERB+	VFG2_ENCODERB+
18	VFG2_GPOUT1_TTL	VFG0_GPIN3-	VFG0_GPIN3-	VFG0_GPIN3-	VFG0_GPIN3-	VFG2_ENCODERB-	VFG2_ENCODERB-
19	VFG3_TRIGGER+	VFG0_GPIN4+	VFG0_GPIN4+	VFG0_GPIN4+	VFG0_GPIN4+	VFG3_TRIGGER+	VFG3_TRIGGER+
20	VFG3_TRIGGER-	VFG0_GPIN4-	VFG0_GPIN4-	VFG0_GPIN4-	VFG0_GPIN4-	VFG3_TRIGGER-	VFG3_TRIGGER-
21	VFG3_TRIGGER_TTL	GND	GND	GND	GND	VFG3_ENCODERA+	VFG3_ENCODERA+
22	VFG3_ENCODERA_TTL	VFG0_GPOUT0+	VFG0_GPOUT0+	VFG0_GPOUT0+	VFG0_GPOUT0+	VFG3_ENCODERA-	VFG3_ENCODERA-
23	VFG3_GPOUT0_TTL	VFG0_GPOUT0-	VFG0_GPOUT0-	VFG0_GPOUT0-	VFG0_GPOUT0-	VFG3_ENCODERB+	VFG3_ENCODERB+
24	VFG3_GPOUT1_TTL	VFG1_GPOUT0+	VFG0_GPOUT1+	VFG1_GPOUT0+	VFG1_GPOUT0+	VFG3_ENCODERB-	VFG3_ENCODERB-
25	GND	VFG1_GPOUT0-	VFG0_GPOUT1-	VFG1_GPOUT0-	VFG1_GPOUT0-	GND	GND
26	GND	VFG0_GPOUT3+	VFG0_GPOUT2+	VFG2_GPOUT0+	VFG0_GPOUT3+	VFG0_CC3+	VFG0_CC3+
27	VFG0_ENCODERA+	VFG0_GPOUT3-	VFG0_GPOUT2-	VFG2_GPOUT0-	VFG0_GPOUT3-	VFG0_CC3-	VFG0_CC3-
28	VFG0_ENCODERA-	VFG0_GPOUT1_TTL	VFG0_GPOUT3_TTL	VFG0_GPOUT1_TTL	VFG0_GPOUT1_TTL	VFG1_CC3+	VFG1_CC3+
29	VFG0_ENCODERB+	GND	GND	GND	GND	VFG1_CC3-	VFG1_CC3-
30	VFG0_ENCODERB-	VFG1_GPOUT1_TTL	VFG0_GPOUT4_TTL	VFG1_GPOUT1_TTL	VFG1_GPOUT1_TTL	VFG2_CC3+	VFG2_CC3+
31	VFG0_GPOUT0+	VFG0_GPOUT2_OC	VFG0_GPOUT5_OC	VFG3_GPOUT0_OC	VFG0_GPOUT2_OC	VFG2_CC3-	VFG2_CC3-
32	VFG0_GPOUT0-	VFG0_GPOUT2_VCC	VFG0_GPOUT5_VCC	VFG3_GPOUT0_VCC	VFG0_GPOUT2_VCC	VFG3_CC3+	VFG3_CC3+
33	VFG0_ENCODERB_TTL	VFG1_GPOUT2_OC	VFG0_GPOUT6_OC	VFG2_GPOUT1_OC	VFG1_GPOUT2_OC	VFG3_CC3-	VFG3_CC3-
34	VFG1_ENCODERA+	VFG1_GPOUT2_VCC	VFG0_GPOUT6_VCC	VFG2_GPOUT1_VCC	VFG1_GPOUT2_VCC	GND	GND
35	VFG1_ENCODERA-	GND	GND	GND	GND	VFG0_TRIGGER_TTL	VFG0_TRIGGER_TTL
36	VFG1_ENCODERB+	GND	GND	GND	GND	VFG0_ENCODERA_TTL	VFG0_ENCODERA_TTL

37	VFG1_ENCODERB-	Reserved	Reserved	Reserved	Reserved	VFG0_ENCODERB_TTL	VFG0_ENCODERB_TTL
38	VFG1_GPOUT0+	GND	GND	GND	GND	VFG1_TRIGGER_TTL	VFG1_TRIGGER_TTL
39	VFG1_GPOUT0-	Reserved	Reserved	Reserved	Reserved	VFG1_ENCODERA_TTL	VFG1_ENCODERA_TTL
40	VFG1_ENCODERB_TTL	GND	GND	GND	GND	VFG1_ENCODERB_TTL	VFG1_ENCODERB_TTL
41	GND	VFG1_TRIGGER+	Reserved	VFG1_TRIGGER+	VFG1_TRIGGER+	VFG2_TRIGGER_TTL	VFG2_TRIGGER_TTL
42	VFG2_ENCODERA+	VFG1_TRIGGER-	Reserved	VFG1_TRIGGER-	VFG1_TRIGGER-	VFG2_ENCODERA_TTL	VFG2_ENCODERA_TTL
43	VFG2_ENCODERA-	VFG1_TRIGGER_TTL	Reserved	VFG1_TRIGGER_TTL	VFG1_TRIGGER_TTL	VFG2_ENCODERB_TTL	VFG2_ENCODERB_TTL
44	VFG2_ENCODERB+	VFG1_ENCODER+	VFG0_ENCODER_B+	VFG1_ENCODER+	VFG1_ENCODER+	VFG3_TRIGGER_TTL	VFG3_TRIGGER_TTL
45	VFG2_ENCODERB-	VFG1_ENCODER-	VFG0_ENCODER_B-	VFG1_ENCODER-	VFG1_ENCODER-	VFG3_ENCODERA_TTL	VFG3_ENCODERA_TTL
46	VFG2_GPOUT0+	VFG1_ENCODER_TTL	VFG0_ENCODER_B_TTL	VFG1_ENCODER_TTL	VFG1_ENCODER_TTL	VFG3_ENCODERB_TTL	VFG3_ENCODERB_TTL
47	VFG2_GPOUT0-	Reserved	Reserved	VFG2_TRIGGER+	Reserved	Reserved	Reserved
48	VFG2_ENCODERB_TTL	Reserved	Reserved	VFG2_TRIGGER-	Reserved	VFG0_CC3_TTL	VFG0_CC3_TTL
49	VFG3_ENCODERA+	Reserved	Reserved	VFG2_TRIGGER_TTL	Reserved	VFG0_CC4_TTL	VFG0_CC4_TTL
50	VFG3_ENCODERA-	VFG0_ENCODER_B+	Reserved	VFG2_ENCODER+	VFG0_ENCODER_B+	VFG0_CC2_TTL	VFG0_CC2_TTL
51	VFG3_ENCODERB+	VFG0_ENCODER_B-	Reserved	VFG2_ENCODER-	VFG0_ENCODER_B-	VFG1_CC3_TTL	VFG1_CC3_TTL
52	VFG3_ENCODERB-	VFG0_ENCODER_B_TTL	Reserved	VFG2_ENCODER_TTL	VFG0_ENCODER_B_TTL	VFG1_CC4_TTL	VFG1_CC4_TTL
53	VFG3_GPOUT0+	Reserved	Reserved	VFG3_TRIGGER+	Reserved	VFG1_CC2_TTL	VFG1_CC2_TTL
54	VFG3_GPOUT0-	Reserved	Reserved	VFG3_TRIGGER-	Reserved	VFG2_CC3_TTL	VFG2_CC3_TTL
55	VFG3_ENCODERB_TTL	Reserved	Reserved	VFG3_TRIGGER_TTL	Reserved	VFG2_CC4_TTL	VFG2_CC4_TTL
56	GND	VFG1_ENCODER_B+	Reserved	VFG3_ENCODER+	VFG1_ENCODER_B+	VFG2_CC2_TTL	VFG2_CC2_TTL
57	VFG0_GPOUT2_TTL	VFG1_ENCODER_B-	Reserved	VFG3_ENCODER-	VFG1_ENCODER_B-	VFG3_CC3_TTL	VFG3_CC3_TTL
58	VFG1_GPOUT2_TTL	VFG1_ENCODER_B_TTL	Reserved	VFG3_ENCODER_TTL	VFG1_ENCODER_B_TTL	VFG3_CC4_TTL	VFG3_CC4_TTL
59	VFG2_GPOUT2_TTL	Reserved	Reserved	Reserved	Reserved	VFG3_CC2_TTL	VFG3_CC2_TTL
60	VFG3_GPOUT2_TTL	VFG1_GPOUT3_TTL	Reserved	VFG3_GPOUT1_TTL	VFG1_GPOUT3_TTL	GND	GND
61	NC	NC	NC	NC	NC	NC	NC
62	NC	NC	NC	NC	NC	NC	NC